RESIDUAL SECOND ORDER INTERMODULATION SUPPRESSION IN THIRD ORDER DISTORTION GENERATORS

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Abstract

Commonly used diode-based third order distortion generators produce residual second order distortion signals due to the unmatched statistical characteristics of the diodes. In this paper, a novel circuit technique is presented by which, in theory, the suppression of undesirable residual second order distortion is achieved. A theoretical analysis of the proposed novel circuit topology was carried out using Volterra series analysis. Simulated results show that the proposed technique posses a residual second order intermodulation distortion (IM2) 35 dB lower than the one obtained with conventional architectures. Experimental results indicate that 20 dB cancellation is achievable.

1. Introduction

Signal predistortion is a widely used linearization technique which has found application in the design of highly linear analog optical transmitters such as the ones used in CATV [1-3] and microwave links [4] as well as in the design of high power amplifiers utilized in wireless communications and microwave radio systems [5]. The technique consists of inserting a set of predistorters before the device to be linearized such that each predistorter generates a non-linearity of fixed order whose amplitudes and phases, in a frequency range, are respectively equal and 180 degrees out of phase to the ones produced by the device to be linearized. As a result, the output signal, ideally, is linear (at least, the output signal does not contain the non-linearity orders of the predistorter). However, in practice, predistorters not only generate the order of the non-linearity for which they were designed but also generate residual non-linearities of different orders. These residual non-linearities may interact with the main non-linearity introduced by another predistorter (in the case that multiple predistorters are used) or add extra non-linearities to the overall circuit, which may have a detrimental effect in the performance of the circuit [1]. For that reason, it is important to design predistorters that reduce, as much as possible, the generation of unwanted non-linearities. In this paper, a novel technique is presented by which the residual second order intermodulation distortion (IM2) of a third order generator is substantially reduced.

Figure 1-(a) shows a general implementation of a third-order predistorter (TOP). It consists of a third order-distortion generator and a pad (implemented by resistors R_1, R_2, and R_3) which is utilized to sample the RF signal from the main path and also to inject the non-linear signal generated by the distortion generator. V_g is the input RF voltage, R_g is the internal resistance of the generator and R_L is the load impedance. Several types of diode-configurations can be utilized to implement the distortion generator. Figures 1(b) and (c) show, respectively, a conventional anti-parallel and a conventional bridge configuration [1,5,6].

The topologies of the circuits are such that when all the diodes are identical only third order distortion is injected to the main path. However, when the diodes are not identical second order non-linearities are generated. The main cause for the unmatched characteristics among diodes of the same type is the dissimilarity of their ideality factors, η. Figure 2 shows the residual IM2 delivered to the load, R_L, by a conventional anti-parallel predistorter configuration utilizing Shottky diodes, as a function of the ideality factor of diode D_2 (η_2). The simulated results shown in the figure were obtained utilizing the software CNL/2 [7] where it was assumed that the ideality factor of diode D_1 (η_1) is equal to one and η_2 changes from 1 to 1.2. Figure 3 shows the Shottky diode model utilized in the simulation [8,9]. R_s, R_j and C_j are, respectively, the series resistance, and the small signal junction resistance and capacitance. For simulation purposes, the effect of C_j was neglected. Table I shows the diodes' parameters, the resistor values of the pad, and the currents and voltages utilized in the simulation. I_B is the dc bias current of the diodes. The sub-index utilized for each of the diodes' parameters indicates with which diode the parameter is associated.

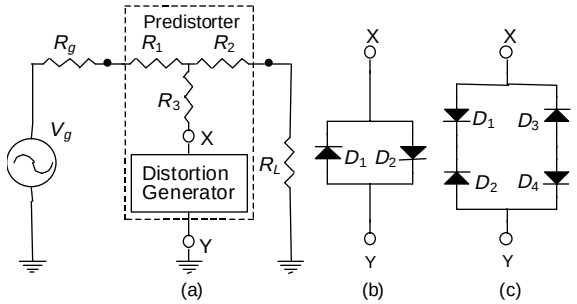

Fig. 1. (a) Third order predistorter configuration, (b) conventional anti-parallel generator, (c) conventional bridge generator. DC bias circuits are not shown.

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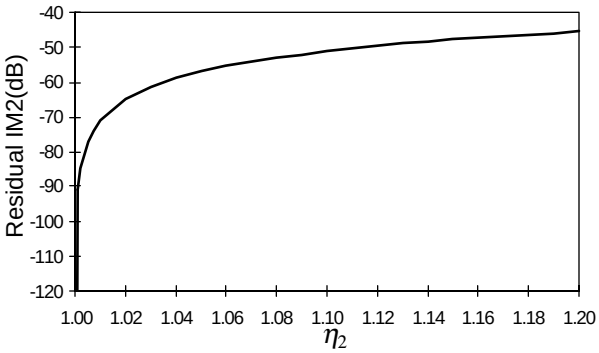

Fig. 2. Residual IM2 as a function of η_2.

It should be noted that the residual IM2 is significantly reduced for values of η_2 smaller than 1.01 and it is completely suppressed when η_2=1. However, for larger values of η_2, the residual IM2 becomes significant. Similar results to those shown in Figure 2 can be obtained for the bridge configuration.

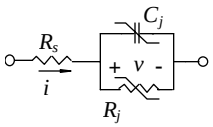

Fig 3. Equivalent circuit for a Schottky diode.

η_1	η_2	R_{S1}	R_{S2}	I_{B1}	I_{B2}
1	1-1.2	5 Ω	5 Ω	1 mA	1 mA
R_g	R_1	R_2	R_3	R_L	V_g
75 Ω	10	10 Ω	80 Ω	75 Ω	0 dBm

Table I. Diodes' parameters, resistor values, currents and voltages used in the simulation.

2. Proposed Solution and Analysis

Figures 4 (a) and (b) show, respectively, two novel circuit topologies that reduce the generation of residual IM2 for the anti-parallel and bridge configurations. The modification to the bridge configuration consists of adding a resistor *R* between the middle nodes of the two branches. Meanwhile, the modified anti-parallel configuration consists of adding two resistors (R_d) to form a bridge configuration in addition to the resistor *R*. In this section, it is shown that by choosing proper resistor values, a substantial reduction of the residual IM2 can be achieved.

The analysis of the circuits shown in Figure 4 is carried out using the method of the non-linear currents based on Volterra series analysis [8]. The modified bridge configuration in Figure 4 (b) is analyzed first since, as it will be shown later, the modified anti-parallel configuration is a particular case of it.

From Figure 3, neglecting the effect of the non-linear capacitance C_j, it can be seen that a Schottky diode can be represented by a linear resistance (R_S) in series with a non-linear resistance (R_j). R_j has voltage *v* across it and current *i*, its current-voltage relation is given by [8]:

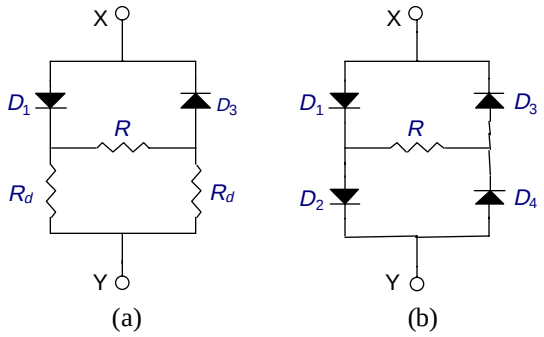

Fig. 4. Proposed new configurations to reduced residual IM2, (a) modified anti-parallel configuration (b) modified bridge configuration. DC bias circuits are not shown.

$$i = g_1 v + g_2 v^2 + g_3 v^3 + \ldots\ldots, \quad (1)$$

where $g_1 = I_B\alpha$, $g_2 = \frac{1}{2} I_B \alpha^2$, $g_3 = \frac{1}{6} I_B \alpha^3$ and $\alpha = \frac{q}{\eta k T}$.

T, *q* and *k* are respectively, the junction temperature, the electron charge, and the Boltzman's constant.

Figures 5 (a) and (b) show, respectively, the equivalent circuits of a Schottky diode utilized to calculate the first- and second-order components using the method of non-linear currents. The voltage v_1, is found through linear analysis, assuming that all sources of non-linearities are set to zero. The second order current source, $i_2 = g_2 v_1^2$, which represent all the second current components in the non-linear element, is found from the voltage v_1 calculated previously. The voltage V_1 is the total linear voltage across the resistor R_s and the conductance g_1, as shown in Figure 5 (a).

Figures 6 (a) and (b) show, respectively, the equivalent circuits for the linear and second order analysis of the TOP using the modified bridge configuration shown in Figure 4 (b). R_e and V_e are, respectively, the equivalent Thevenin's resistance and voltage between nodes X and Y, *b*=1/*R* and

$$a_k = \frac{g_{1k}}{(g_{1k} R_{Sk} + 1)}, \quad (2)$$

$$V_{1k} = (g_{1k} R_{Sk} + 1) v_{1k}, \quad (3)$$

$$I_{2k} = \frac{i_{2k}}{g_{1k} R_{Sk} + 1} = \frac{g_{2k} v_{1k}^2}{g_{1k} R_{Sk} + 1} = \frac{g_{2k} V_{1k}^2}{(g_{1k} R_{Sk} + 1)^3}, \quad (4)$$

where the sub-index *k*=1,2,3,4 is associated with the diode numbers as indicated in Figure 4(b).

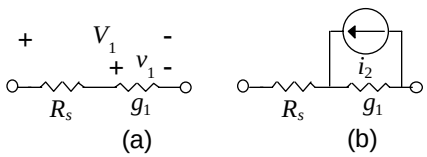

Fig. 5. (a) Linear equivalent circuit and (b) second order equivalent circuit used to calculate the linear and second order components using the method of non-linear currents.

From Figure 6 (a), it can be seen that each of the voltages V_{1k} can be expressed as a function of the linear output voltage, $V_o^{(1)}$ as follows:

$$V_{11} = \frac{b(a_2 + a_4) + a_2(a_3 + a_4)}{\xi} V_O^{(1)}, \quad (5)$$

$$V_{12} = \frac{b(a_1 + a_3) + a_1(a_3 + a_4)}{\xi} V_O^{(1)}, \quad (6)$$

$$V_{13} = \frac{b(a_2 + a_4) + a_4(a_1 + a_2)}{\xi} V_O^{(1)}, \quad (7)$$

$$V_{14} = \frac{b(a_1 + a_3) + a_3(a_1 + a_2)}{\xi} V_O^{(1)}, \quad (8)$$

where

$$\xi = b(a_1 + a_2 + a_3 + a_4) + (a_1 + a_2)(a_3 + a_4). \quad (9)$$

The voltage $V_o^{(1)}$, in turn, can be calculated as a function of V_e as follows:

$$V_O^{(1)} = \frac{V_e}{1 + R_e\left\{\frac{a_1[b(a_1+a_2)+a_2(a_3+a_4)] + a_3[b(a_2+a_4)+a_4(a_1+a_2)]}{\xi}\right\}}, \quad (10)$$

The voltage $V_o^{(2)}$ indicated in Figure 6 (b) represent the second order output voltages and it can be found, after a tedious process, to be:

$$V_O^{(2)} = \frac{-[a_2(b + a_3 + a_4) + ba_4]\, I_{21} + [a_1(b + a_3 + a_4) + ba_3]\, I_{22} + [a_4(b + a_1 + a_2) + ba_2]\, I_{23} - [a_3(b + a_1 + a_2) + ba_1]\, I_{24}}{a_1[a_2(b + a_3 + a_4) + ba_4] + a_3[a_4(b + a_1 + a_2) + ba_2] + \frac{\xi}{R_e}}, \quad (11)$$

Note that the voltage $V_o^{(2)}$ can be calculated as a function of the voltage generator by using Equations (4), (5), (6), (7), (8) and (10).

From Eq. (11), it can be seen that $V_o^{(2)}$ is reduced to zero when the numerator is equal to zero. A value of b (=1/R) can be found that satisfies $V_o^{(2)} = 0$. This indicates that complete cancellation of the second order distortion can be obtained even though the diodes have different ideality factors. Also, it should be noted that when all diodes are equal, the presence of the conductance b, does not affect the cancellation of the second order distortion.

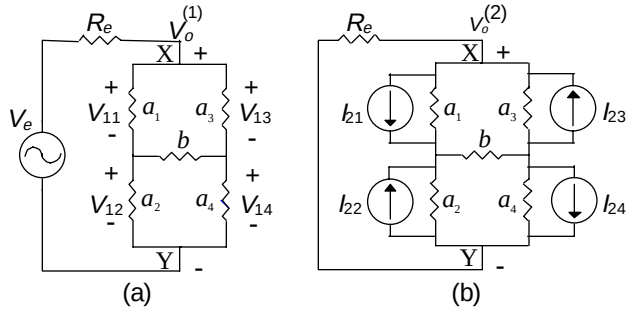

Fig.6. (a) Linear and (b) second order equivalent circuits for the bridge configuration using the methods of non-linear currents.

(a) Modified Anti-Parallel Distortion Generator

For this particular case, the model shown in Figure 6 can be applied to analyze the modified anti-parallel distortion generator by setting I_{22}=I_{24}=0 and a_2=a_4=1/R_d. By equating $V_o^{(2)} = 0$, a value of R can be found as follows:

$$R = \frac{2[a_1^{2/3}(a_3R_s + 1) - a_3^{2/3}(a_1R_s + 1)]}{a_3^{2/3}\left[\frac{1}{R_d}(a_1R_s + 1) + a_1\right] - a_1^{2/3}\left[\frac{1}{R_d}(a_3R_s + 1) + a_3\right]}. \quad (12)$$

R_d should be selected such that $R > 0$. Also, R_d should not be too large since, in that case, the third order intermodulation distortion (IM3) is substantially reduced in comparison to the one of the conventional configuration.

Figure 7 shows the residual IM2s (at R_L) as a function of η_2 when the TOP is utilized in conjunction with the modified anti-parallel distortion generator and the conventional one. For both cases the parameters shown in Table I were utilized in the simulation. For the modified anti-parallel configuration, R_d=60Ω and R=686Ω. The value of R was calculated using Eq. (12) and assuming that η_1=1 and η_2=1.2. It should be noted that for the anti-parallel configuration, the residual IM2 is suppressed when η_2 is 1 and 1.2. Moreover, if η_2 <1.2, and the resistor R is kept unchanged, the residual IM2 of the modified anti-parallel configuration is at least 35 dB smaller than the residual IM2 corresponding to the conventional configuration. The penalty in adding the resistors R and R_d is a 1.5 dB reduction of the IM3 delivered to the load in comparison to the one delivered by a conventional anti-parallel configuration under similar conditions. However, in most cases, this penalty can be easily compensated by biasing the diodes at a lower current or by increasing the input signal power.

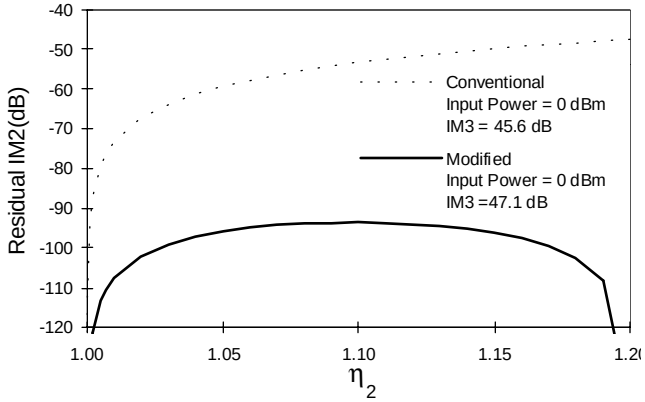

Fig 7. Simulation results for the (a) conventional and (b) modified anti-parallel configuration.

(b) Modified Bridge Distortion Generator

Given a set of diodes, the residual IM2 of the conventional bridge configuration is maximum when the selected diodes satisfy the following conditions: $\eta_1=\eta_4$, $\eta_2=\eta_3$, $\eta_1\neq\eta_2$ where η_1 and η_2 are, respectively, the maximum and minimum ideality factors of the set or vice versa. Under those conditions, $a_1= a_4$, $a_2= a_3$, $b_1= b_4$, $b_2= b_3$, $I_1=I_4$, and $I_2= I_3$. By equating $V_o^{(2)}=0$ results:

$$R=\frac{a_1^{2/3}(a_2R_s+1)-a_2^{2/3}(a_1R_s+1)}{a_1a_2^{2/3}-a_2a_1^{2/3}}. \qquad (13)$$

It is important to mention that the optimum value of R depends on the bias currents of the diodes since the parameter a_k (k=1,2,3,4) depends on the bias current of diode D_k. It is interesting to consider the case when the series resistance of the diodes is set to zero. For this case, Eq. (13) is reduced to:

$$R=r_1^{1/3}r_2^{2/3}+r_1^{2/3}r_2^{1/3}, \qquad (14)$$

where $r_1 = 1/g_{11}$, and $r_2 = 1/g_{12}$. Since, $r_1\approx r_2=r$, it can be concluded that

$$R\approx 2r. \qquad (15)$$

Equation (15) indicates that the resistor R is approximately equal to twice the incremental resistance of the diodes ($1/g_{1k}$). This suggests that R can be implemented by two diodes (identical to the ones used in the bridge) in series and under the same bias conditions as the other diodes that form the bridge. Consequently, if R is implemented by two diodes, the modified bridge configuration can work over a range of bias currents. Figure 8 shows the residual IM2 as a function of the diodes' bias current, using the TOP with the modified bridge configuration in which the resistor R is implemented by two diodes in series of the same type to the ones utilized in the bridge. Results are presented for different ideality factors of the diodes that implement R. For comparison purposes, the residual IM2 as a function of the diodes' bias current for the TOP with a conventional bridge configuration is also shown in the figure. For the simulation results shown in Figure 8, it is assumed that diodes D_1 and D_4, as well as diodes D_2 and D_3, are identical. The parameters shown in Table I were used for the simulation (η_1=1 and η_2=1.2). It can be observed that for low bias currents, the residual IM2 of the modified bridge configuration is about 25 dB better than that of the conventional configuration. At higher currents, the improvement is reduced to about 10 dB. This is due to the fact that the values of the incremental resistance of the diodes at high bias currents are of the same order of magnitude to their series resistors. Correspondingly, for high bias currents Eq. (15) is not completely accurate. However, in many applications, the bias currents are normally low since high IM3 are required. For these applications, the possibility of implementing the resistor R using two diodes in series is very attractive.

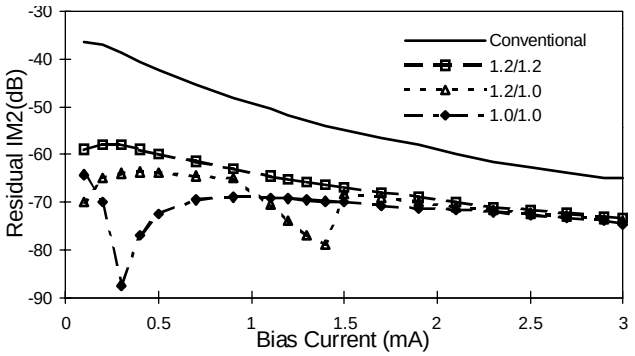

Fig. 8. Residual IM2 of the bridge configuration as a function of the bias current of the diodes for the case that the resistor R is implemented by two Schottky diodes.

3. Experimental Results

Two TOPs were implemented: one using the conventional anti-parallel configuration and the other using the modified version. For both cases, the same pair of HP HSMS2820 Schottky diodes were utilized to implement the circuits. The measured characteristic of the diodes were those shown in Table I. D_2 has an ideality factor η_2=1.2. The residual IM2 of the modified configuration was 20 dB lower than the one measured for the conventional one. For the modified configuration R_d=47 Ω and R=180 Ω. I_B was set to 1.5 mA. For the measurements, the fundamental frequencies were set to f_1=7 MHz and f_2=25 MHz. IM2 was measured at 18 MHz and 32 MHz.

Conclusion

In this paper, a novel technique was presented that reduces the generation of residual IM2 in third order predistorters using anti-parallel and bridge configurations. It was shown, that, in theory, the residual IM2 can be completely canceled even though the diode ideality factors are different. Experimental results showed that substantial reduction of IM2 can be achieved. Moreover, a novel topology was proposed that may substantially suppressed the residual IM2 for different bias conditions.

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